

FIG. 1

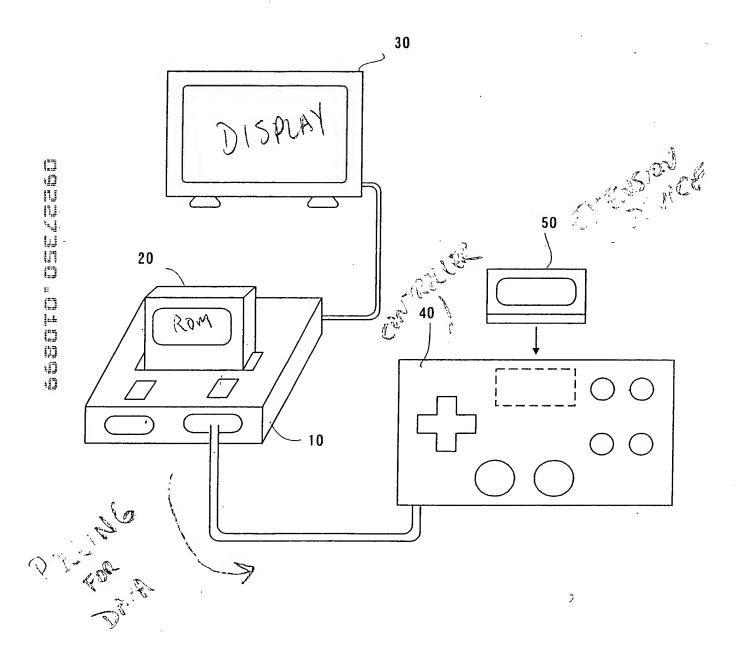


FIG. 2

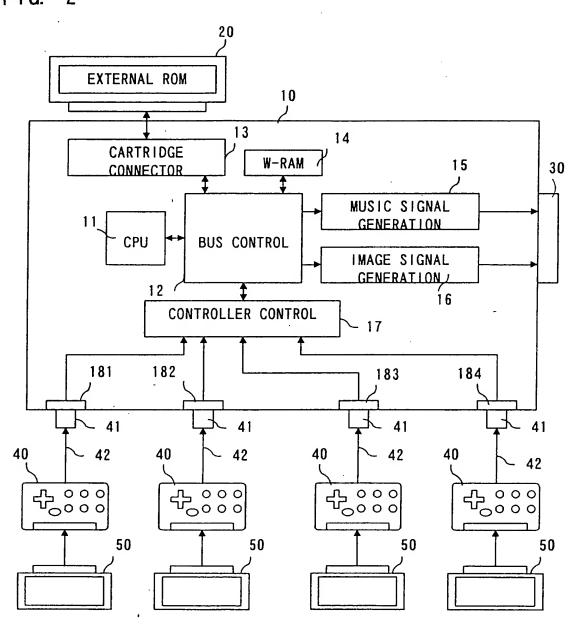


FIG. 3

CPU MEMORY MAP

201	IMAGE DATA REGION	
	PROGRAM DATA REGION	EXTERNAL MEMORY AREA
<u>202</u>	•	
<u>141</u>	CONTROLLER DATA REGION	W-RAM AREA

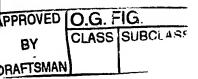
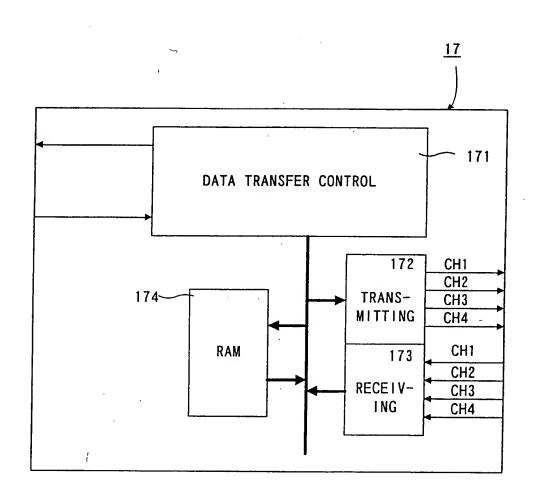


FIG. 4



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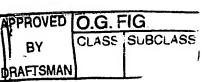
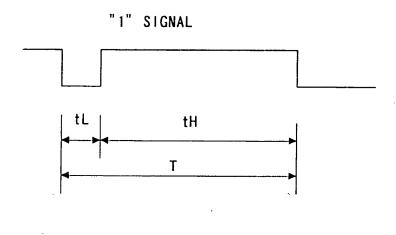


FIG. 5



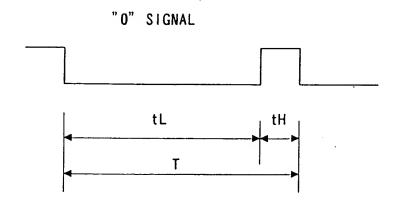


FIG. 6

RAM 174

RAM 1/4	
1CH COMMAND STORAGE	
POSITION 174a	
1714	
1CH TRANSMISSION/RECEPTION	
DATA STORAGE POSITION	
174b	
2CH COMMAND STORAGE	
POSITION 174c	
	_
2CH TRANSMISSION/RECEPTION	
DATA STORAGE POSITION	
174d	
3CH COMMAND STORAGE	
POSITION 174e	
1	
3CH TRANSMISSION/RECEPTION	
DATA STORAGE POSITION	
174f	
4CH COMMAND STORAGE	
POSITION 174g	
100111011	
4CH TRANSMISSION/RECEPTION	
DATA STORAGE POSITION	
174h	

FIG. 7

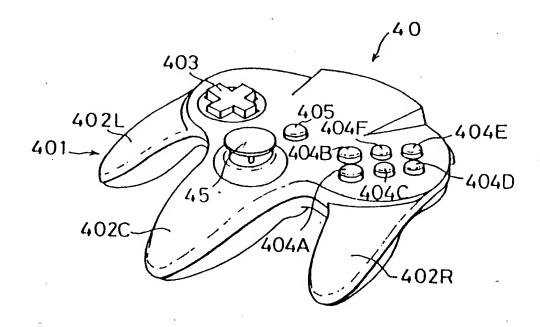


FIG. 8

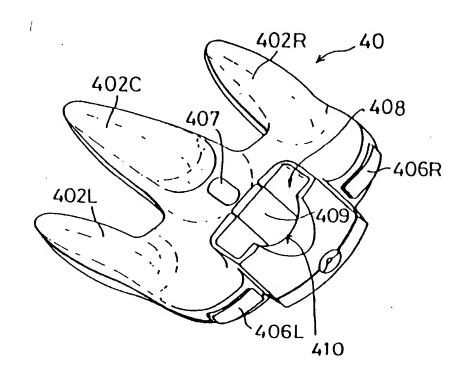




FIG. 9

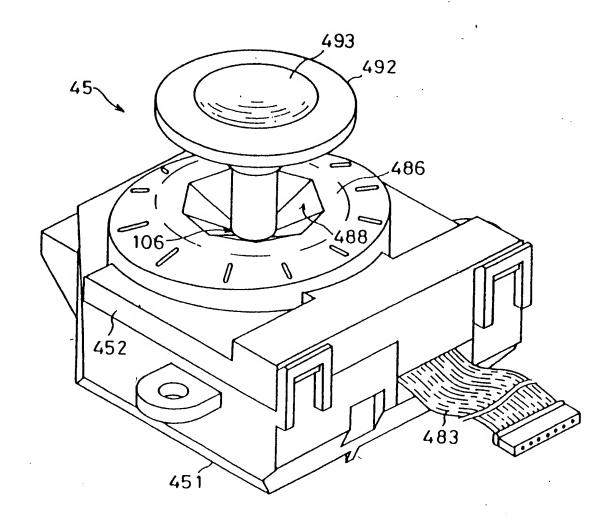
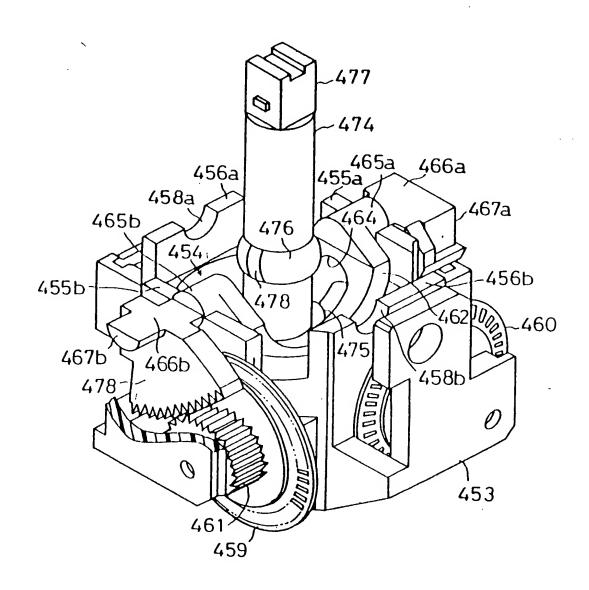


FIG. 10



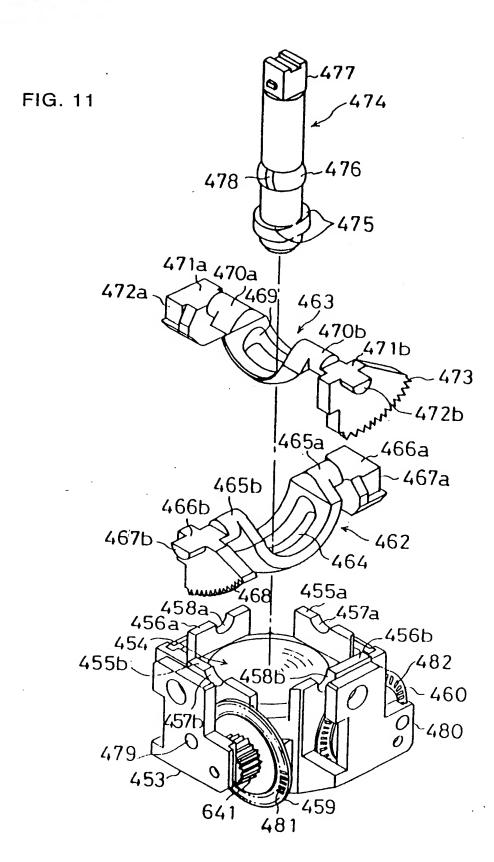


FIG. 12

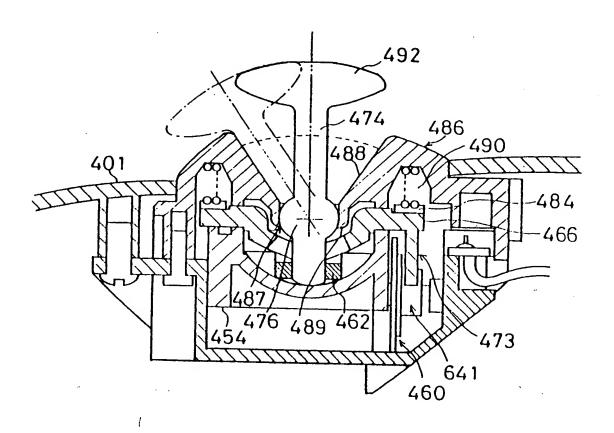


FIG. 13

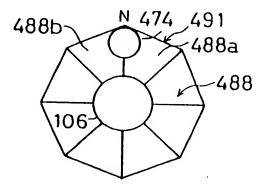




FIG. 14 <u>40</u> 44 444 2-SHAFT **PULSE** 444Y COUNTER COUNTER COUNTER 442 45 444X 445 43 RESET - 42 CONVER-TRANSMI-448 TTING SION C 0 POWER N ON COMMAND T RESET RESET PIN RESET R RECEIV-0 ING 443 447 RESET L LEFT ► SW RIGHT -441 RESET START SW. SIGNAL DETECTION 403 - 407 JOYPORT CONTROL 446 46 AD-<u>50</u> RD/WR/CS **DATA DRESS** 51 52 RAM

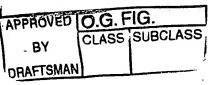


FIG. 15

1 BYTE	В	A	G	START	↑	1	-		
2 BYTE	JSRST	0	L	R	E	D	С	F	
3 BYTE	X ORDINATE								
4 BYTE	Y ORDINATĒ								

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APPROVED O.G. FIG. CLASS SUBCLASS



FIG. 16

COMMAND O: TRANSMITTING TYPE OF CONTROLLER RECEPTION: 1 BYTE TRANSMISSION: 3 BYTES

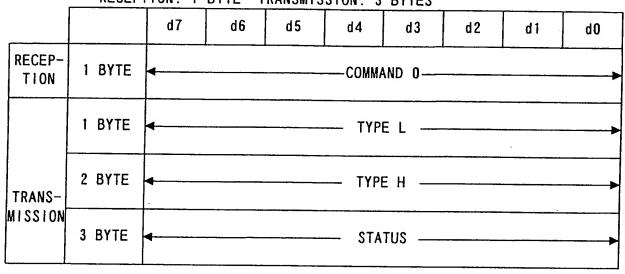
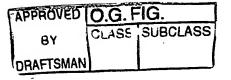


FIG. 17

COMMAND 1: ACCESSING STANDARD CONTROLLER RECEPTION: 1 RATE TRANSMISSION, A DATES

	KECE	PITON: I	BAIF	IKANSMI	2210N:	4 BYTES					
		. d7	d6	d5	d4	d3	d2	d1	d0.		
RECEP- TION	1 BYTĘ	4	COMMAND 1								
TRANS-	1 BYTE	В	Α	G	START	- 1	↓ ·	-			
	2 BYTE	JSRST*	0	L	R	Е	D	С	F		
	3 BYTE	X ORDINATE									
	4 BYTE	Y ORDINATE									

* HIGH LEVEL WHEN L, R AND START BUTTONS ARE SIMULTANEOUSLY DEPRESSED



ng prominent and the company of the

FIG. 18

COMMAND 2: READ-OUT RAM RECEPTION: 3 BYTES TRANSMISSION: 33 BYTES ď d7 d5 **d6 d4 d** 3 d2 **d1** 0 COMMAND2 -1 BYTE 2 BYTE ----- ADDRESS H -----RECE-PTION ----- ADDRESS CRC -3 BYTE ← ADDRESS L → ---- DATA 0 ----1 BYTE 2 BYTE ——— DATA 1 — TRAN-SMIS-SION _____ DATA 31 ____ 32 BYTE ► DATA CRC — 33 BYTE ◄



FIG. 19

COMMAND 3:

WRITE TO RAM

RECEPTION: 35 BYTES TRANSMISSION: 1 BYTES

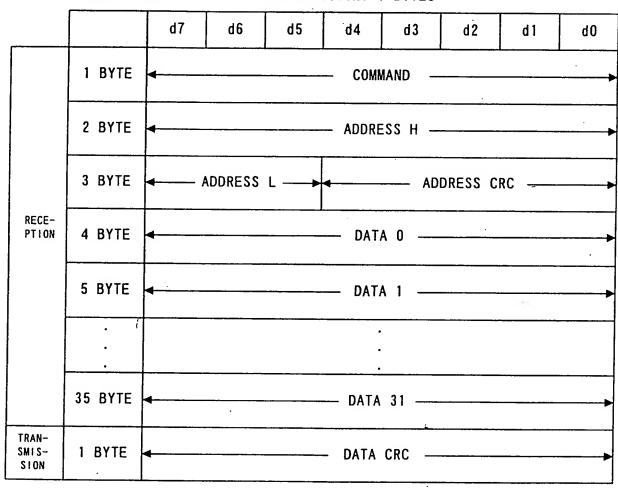
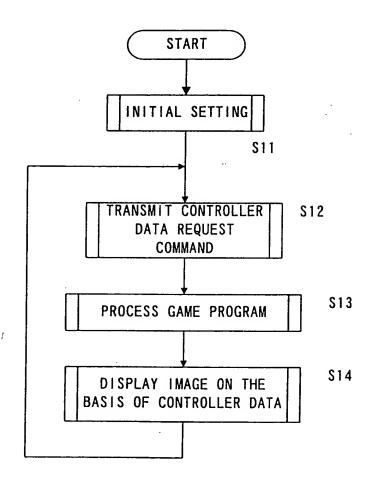
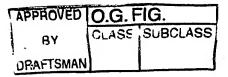


FIG. 20



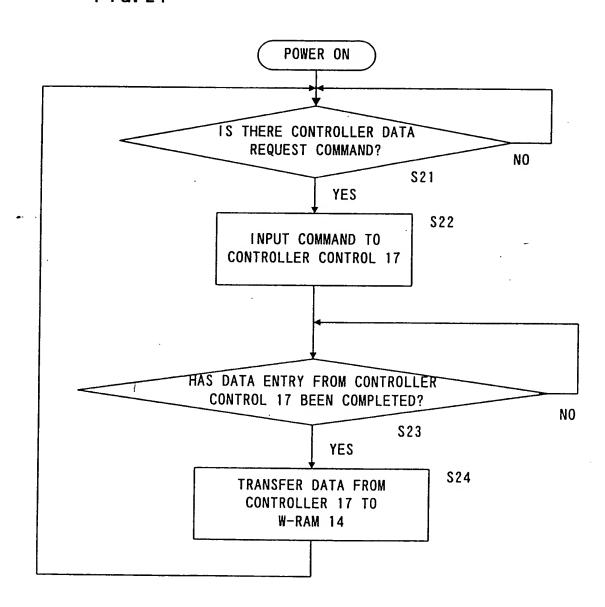
the time that had been men and the time time the time time that the time time that

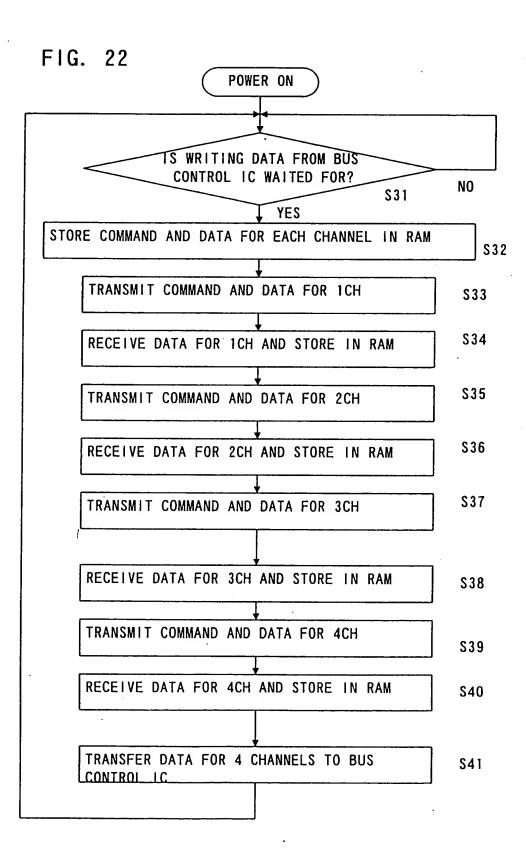


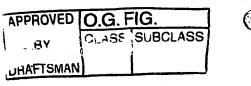
der the state of term trees on and the first that the trees the tr

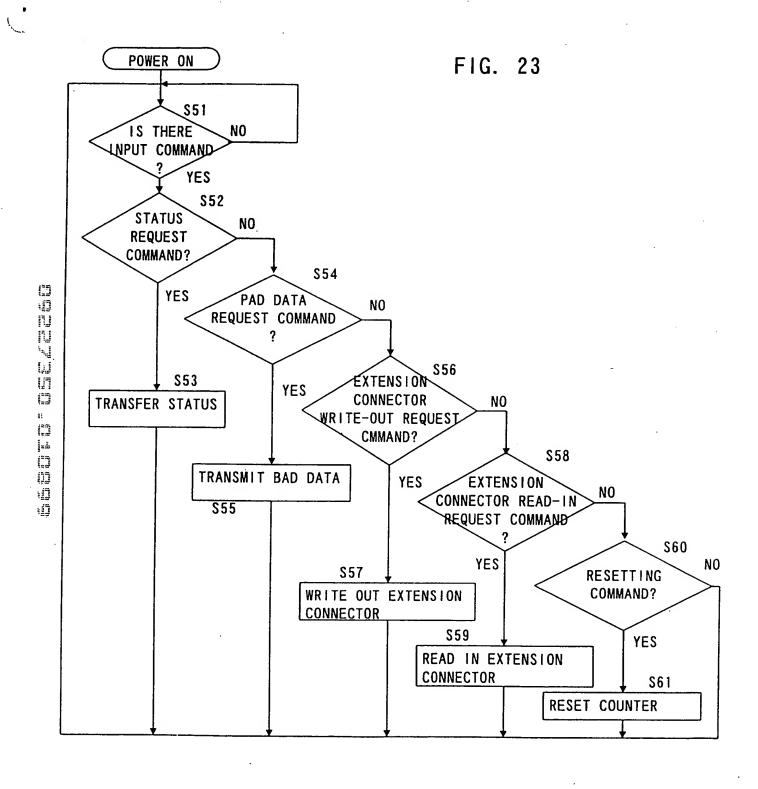
fron, fron, 4..... er 11 m m and 4.... fron, fron, 4.... er 11 m m and 4.... fron fron 4... er 11 m and 4...

FIG. 21









TOPPEN HINDS

FIG. 24

COMMAND 255: CONTROLLER RESETTING

RECEPTION: I BYTE TRANSMISSION: 3BYTE										
		d7	d6	d5	d4	d3	d2	d 1	d0	
RECEP- TION	1 BYTE	4	COMMAND 255							
TRANS- MISSION 1 BYTE TYPE L										
100101	2 BYTE	▼ TYPE H ———								
	3 BYTE	4			STA	rus —				

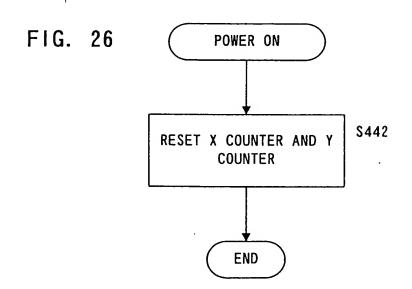


POWER ON

S432

HAVE L, R AND START BUTTONS
SIMULTANEOUSLY DEPRESSED?

RESET X COUNTER AND Y
COUNTER



APPROVED O.G. FIG

BY CLASS SUBCLASS

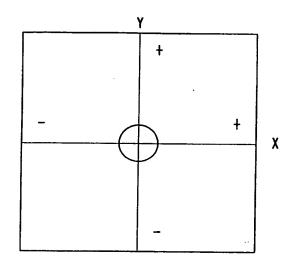
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FIG. 27

PHYSICAL COORDINATE OF JOYSTICK



DISPLAY SCREEN

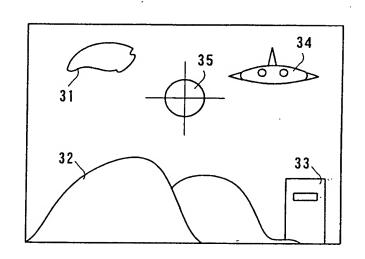
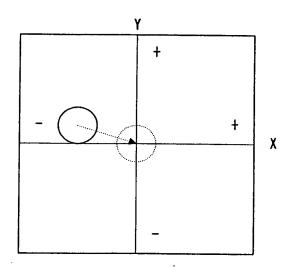


FIG. 28

PHYSICAL COORDINATE OF JOYSTICK



DISPLAY SCREEN

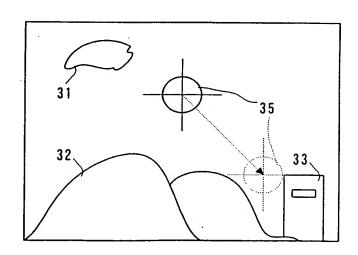




FIG. 29

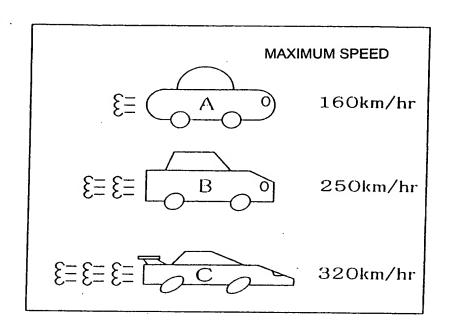


FIG. 30

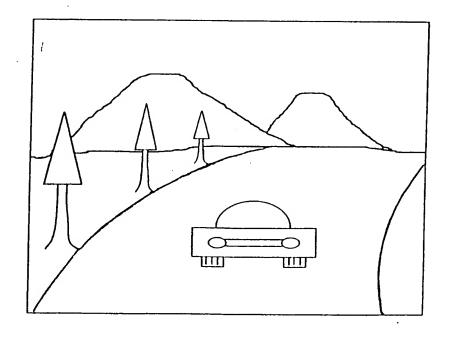
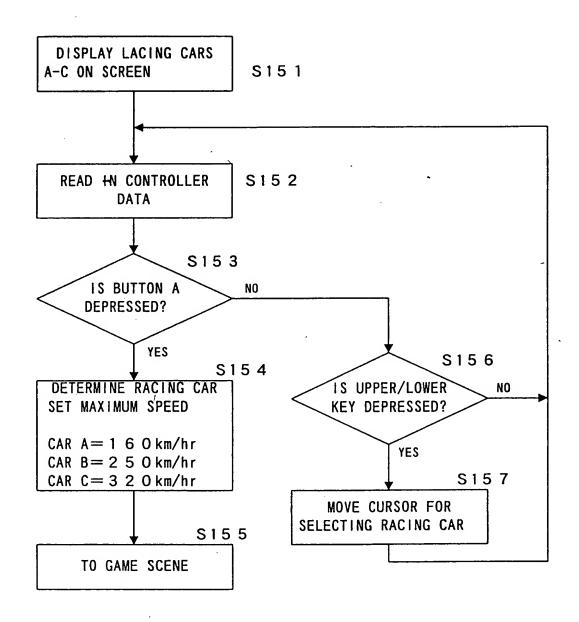
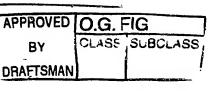


FIG. 31

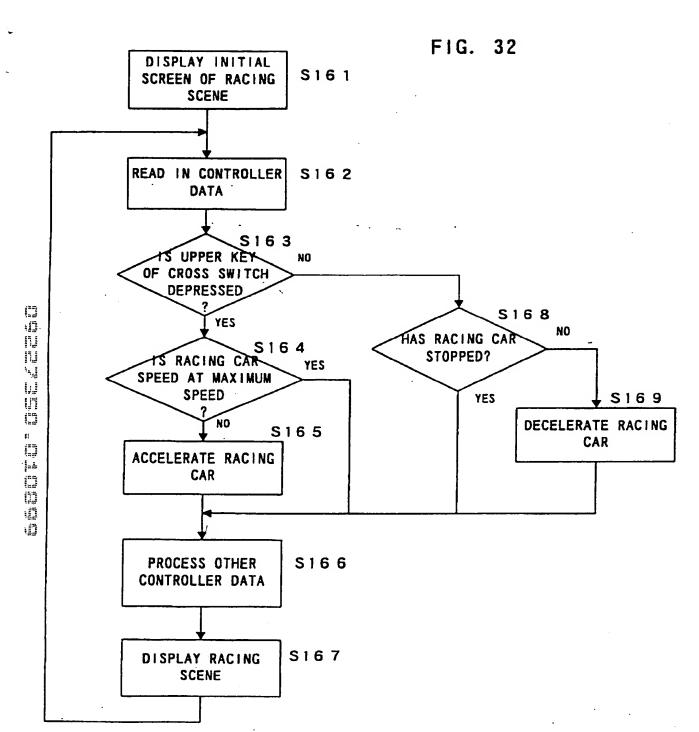


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FIG. 34

